SRAM CELL

Related Applications

[0001] This utility application claims priority to United States Patent Application Serial No. 10/631,169 filed July 3, 2003 and entitled Multi-Configurable Independently Double-Gated MOSFET and is hereby incorporated by reference.

Technical Field

[0002] The present invention relates to the composition and manufacture of a memory and, more specifically, to a random access memory cell.

Background of the Invention

[0003] Random access memory (RAM) provides the temporary storage of information for today's personal computers and mainframes. As such, RAM is a necessary resource for performing computations and the amount of RAM effects the computing processing capability of any system. Each RAM component includes a number of cells or storage locations that can either hold an active or an inactive state that is referred to as a bit. A bit represents the active or inactive state with a 1 or 0, and is the smallest amount of information used by a computer.

[0004] RAM cells are combined into a large array that is used to store vast amounts of information translated binarily by computers. The RAM cells are arranged in specific groups organized in terms of Rows and Columns, with each cell having a specific Row/Column reference that is an address location.

[0005] Dynamic Random-Access Memory (DRAM) is a common form of RAM, with each DRAM cell having a capacitor and a transistor. Over time, the capacitor loses its charge, and the loss of charge results in the loss of information. It is necessary to recharge (refresh) the state in which the cell exists.

[0006] Static random access memory (SRAM) is an improved architecture over DRAM. The term "static" is derived from the fact that it does not need to be refreshed as does DRAM. SRAM requires no refresh and will maintain its information so long as it has sufficient power. This is due to the fact that internally, the SRAM cell includes flip-flop circuitry that does not require refreshing.

[0007] SRAM is also faster and more reliable than DRAM. SRAM can be used alongside the processor as cache while it performs other duties. SRAM speeds allow quicker accesses in comparison to DRAM which must wait several processor clock cycles before providing the needed information. By way of example, DRAM supports access times of about 60 nanoseconds while SRAM can support access times even lower than 10 nanoseconds. Furthermore, the SRAM cycle time is much shorter than that of DRAM, because the SRAM does not need to pause between accesses.

[0008] Unfortunately, the flip-flop circuitry may require four to six transistors that increase the size of the SRAM. The SRAM is unable to compete with the densities found in the DRAM. The density disparity substantially increases the price for SRAMs. Due to the high cost, SRAM is often used only as a memory cache.

[0009] A key concern in memory components is being able to generate smaller devices that consume less power. Although significant progress has been made in this area, a common problem with transistors is the gate voltage control of the channel as the device decreases in size. Gate voltage control is achieved by

exerting a field effect on the channel. As the transistor size decreases, short-channel effects become more problematic and interfere with the gate voltage's ability to provide exclusive channel control. Ideally, total control of the channel should rest with the gate voltage.

[0010] Thus, it would be an advancement in the art to provide a SRAM cell with improved density, superior gate control, and efficient fabrication techniques. Such a device is disclosed and claimed herein.

Brief Description of the Drawings

[0011] A more particular description of the invention briefly described above will be rendered by reference to the appended drawings. Understanding that these drawings only provide information concerning typical embodiments of the invention and are not therefore to be considered limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings, in which:

[0012] Figure 1 is a cross-sectional view of an embodiment of a transistor of the present invention;

[0013] Figure 2 is an isometric view of the transistor of Figure 1;

[0014] Figure 3 is a cross-sectional view of the width of the transistor of Figure 1 along line 3-3;

[0015] Figure 4 is a cross-sectional view of the width of an alternative embodiment of a transistor;

[0016] Figure 5 is a cross-sectional view of the width of an alternative embodiment of a transistor;

[0017] Figure 6 is a schematic representation of the embodiment of Figure 3;

[0018] Figure 7 is a schematic representation of the embodiment of Figure 4;

[0019] Figure 8 is a schematic representation of the embodiment of Figure 5;

[0020] Figure 9 is a cross-sectional view of an alternative embodiment of a transistor of the present invention;

[0021] Figure 10 is a cross-sectional view of an alternative embodiment of a transistor of the present invention;

[0022] Figure 11 is a cross-sectional view of an alternative embodiment of a transistor of the present invention;

[0023] Figure 12 is a cross-sectional view of layers used in the fabrication of the transistor of Figure 1;

[0024] Figure 13 is a cross-sectional view of the device of Figure 12 after formation of a trench;

[0025] Figure 14 is a cross-sectional view of the device of Figure 13 device after formation of doped sidewalls;

[0026] Figure 15 is a cross-sectional view of the device of Figure 14 after removal of the doped sidewalls and formation of a gate insulator;

[0027] Figure 16 is a cross-sectional view of the device of Figure 15 after formation of spacers;

[0028] Figure 17 is a cross-sectional view of the device of Figure 16 after formation of a bottom gate;

[0029] Figure 18 is a cross-sectional view of the device of Figure 17 after formation of a top gate;

[0030] Figure 19 is a cross-sectional view of the device of Figure 18 after formation of a first local interconnect and an ILD layer;

[0031] Figure 20 is a cross-sectional view of the device of Figure 19 after formation of contacts;

[0032] Figure 21 is a schematic diagram of an embodiment of an SRAM cell in accordance with the present invention; and

[0033] Figure 22 is a schematic diagram of an alternative embodiment of an SRAM cell in accordance with the present invention.

Detailed Description of Preferred Embodiments

[0034] Reference is now made to the figures in which like reference numerals refer to like elements. For clarity, the first digit or digits of a reference numeral indicates the figure number in which the corresponding element is first used.

[0035] Throughout the specification, reference to “one embodiment” or “an embodiment” means that a particular described feature, structure, or characteristic is included in at least one embodiment of the present invention. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment.

[0036] Furthermore, the described features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. Those skilled in the art will recognize that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or not described in detail to avoid obscuring aspects of the invention.

[0037] The SRAM cell of the present invention includes unique double-gated transistors that are embodied as discussed in reference to Figures 1 to 20. Referring to Figure 1, a cross-sectional view of one embodiment of the double-gated transistor 10 of the present invention is shown. The illustrated transistor 10 discussed herein is an N-channel device, but may as well be embodied as a P-channel device as can be appreciated by one of skill in the art. The transistor 10 includes a substrate 12

that may be formed of any number of suitable materials. The substrate 12 may include silicon and a buried insulator such as silicon dioxide which is commonly referred to as a buried oxide layer.

[0038] A bottom gate 14 is disposed on the substrate 12 and includes a low resistance doped silicon material. The bottom gate 14 is highly doped, such as by ion implantation, to create a P+ bottom gate in the N-channel configuration. The transistor 10 includes a high resistivity layer 16 that serves as a gate insulation layer. The high resistivity layer 16 may include silicon on insulator (SOI) that is preferably a P-type material. The high resistivity layer 16 may be formed by any number of available methods including SmartCut bonded, SIMOX, metal-induced polyrecrystallization, and so forth.

[0039] The source 18, drain 20, and channel 22 form a current flow path in accordance with MOSFET practice. The source 18 and drain 20 may be formed of any suitable N+ materials in an N-channel configuration. Formation of the source 18 and drain 20 may include deposition of an additional material layer or doping of the existing high resistivity layer 16.

[0040] In a depletion type MOSFET, the channel 22 may include a layer of material that is the same as the source 18 and drain 20, such as an N-type material in the given example. The gate voltage can reduce the channel current by depleting carriers or increase the channel current by increasing carriers. In an enhancement type MOSFET, the channel 22 is an area extending into the P-type material of the high resistivity layer 16. Application of a positive gate voltage pushes away the holes in the P-type material and attracts the moveable electrons in the N-type source 18 and drain 20 to form a channel 22. In Figure 1, the channel 22 is defined as the area between the source 18, drain 20, bottom gate 14, and gate dielectric insulator

28. The channel 22 may therefore be an undoped region of the high resistivity layer 16. As can be appreciated, the present invention is applicable to either depletion or enhancement type MOSFETs.

[0041] The source 18 includes a main body 23 that represents the majority of the source 18 and a source extension 24 that extends from the main body 23 to couple with the channel 22. The source extension 24 has significantly less cross-sectional area than the main body 23. Similarly, the drain 20 includes a main body 25, that is the majority of the drain 20, and a drain extension 26 that extends from the main body 25 and couples to the channel to enable electron flow. The drain extension 26 has significantly less cross-sectional area than the main body 25.

[0042] The extensions 24, 26 increase the distance of the main bodies 23, 25 from the channel 22 to reduce the short-channel effect created by the drain 20. However, in reducing the short-channel effect, a resistance is created in the extensions 24, 26. This is acceptable, given the superior gate control enabled by the reduced field effect. The extensions 24, 26 may be configured in various shapes in coupling to the main bodies 23, 25 to the channel 22. The extensions 24, 25 may also be formed in accordance with various techniques such as by implantation, sidewall spacer methods, or other methods known in the art.

[0043] A gate dielectric insulator 28 is disposed on the channel 22 and a top gate 30 is disposed on the gate dielectric insulator layer 28. The gate dielectric insulator 28 is a dielectric, such as silicon dioxide, that insulates the top gate 30 from the channel 22 as is well known in MOSFET architecture. The top gate 30 may be formed of any suitable metallic material such as Mo, W, Al, or TiN. A local interconnect 32 is disposed on the top gate 30 and may include any number of various materials, including Al.

[0044] The transistor 10 further includes polish stop pad layers 34, 36 that are disposed on the source 18 and drain 20 respectively. The pad layers 34, 36 are formed of a dielectric material. Extending through each pad layer 34, 36 is one or more contact layers 38, 40 that couple to a respective source 18 and drain 20. An interlevel dielectric (ILD) layer 42 is disposed on the pad layer 34, 36 and also has the contact layers 38, 40 extending through to enable contact. The contact layers 38, 40 need only extend through the pad layers 34, 36 where it is necessary to contact the source 18 and drain 20.

[0045] First and second spacers 44, 46 are disposed within to prevent contact between the top gate 30 and the source 18 and drain 20 as shown. The spacers may include any number of insulating materials such as silicon nitride or silicon oxide. The spacers 44, 46 further extend to prevent contact between the local interconnect 32 and the source and drain 18, 20.

[0046] As illustrated, the majority of the source 18 and drain 20 is disposed on one side of a corresponding spacer 44, 46. The source and drain extensions 24, 26 extend proximate to the spacers 44, 46 and couple to the channel 22. The disposition of the spacers 44, 46 and the extensions 24, 26 shield the channel 22 from the field effect of the source and drain 18, 20 while still providing contact to enable electron flow. As transistor size is reduced, the source and drain voltages interfere with the gate voltage and inhibit gate control of the channel 22. The present invention provides improved gate control of the channel 22 by limiting the field effect and capacitance of drain 20 voltages.

[0047] In one implementation, the pads 34, 36 include a different dielectric material than that of the spacers 44, 46. Thus, if the spacers 44, 46 are formed of a

silicon nitride then, the pads 34, 36 are formed of silicon oxide. Conversely, if the pads 34, 36 include a silicon nitride, then the spacers 44, 46 include silicon oxide.

[0048] The transistor 10 further includes third and fourth spacers 48, 50, formed of the same insulating material of the first and second spacers 44, 46. The third and fourth spacers 48, 50 extend vertically along the peripheral edges of the transistor 10. The spacers 48, 50 serve to isolate the transistors 10 from each other and provide radiation resistance and may be referred to as exterior spacers. As can be appreciated, the spacers 48, 50 may extend, alone or in conjunction with other spacers, to surround the components of the transistor 10. An insulating layer 52, such as a STI oxide, may further be disposed around the transistor 10 to provide further isolation. The transistor 10 is encapsulated within the insulating layer 52, spacers 48, 50, and ILD layer 42 to optimize performance.

[0049] The transistor architecture of the present invention provides a four-terminal device that allows the source 18, drain 20, bottom gate 14, and top gate 30 to be biased independently. The bottom gate 14 and the top gate 30 may be wired out to the left or right based on design constraints. Additional conducting and dielectric layers may be disposed on the transistor 10 based on design configurations.

[0050] Referring to Figure 2, an isometric view of the transistor 10 illustrates the upper surface of the ILD layer 42. As shown, the contact layers 38, 40 extend through the ILD layer 42 to enable access to the source 18 and drain 20. The contact layers 38, 40 may provide any number of accesses to the source 18 and drain 20 based on design preferences.

[0051] Referring to Figure 3, a cross-sectional view of the transistor 10 taken along length 3-3 illustrated in Figure 1 is shown. The transistor 10 is a four terminal, double-gated device with each gate having an independent bias. The substrate 12,

bottom gate 14, channel 22, gate dielectric insulator 28, top gate 30, conducting layer 32, and ILD layer 42 are shown vertically disposed relative to one another. Further shown is a second local interconnect 60 that couples to the bottom gate 14 and provides an independent bias to the bottom gate 14. The second local interconnect 60 is the same material as the first local interconnect 32. The first and second local interconnects 32, 60 together provide the local interconnect for the top and bottom gates 14, 30.

[0052] The second local interconnect 60 is separated from the first local interconnect 32 by an STI insulator 62. The insulator 62 may be formed of any suitable material such as an oxide or nitride. In this manner, the top gate 30 and the bottom gate 14 are independently biased. As shown, the top gate 30 is offset relative to the bottom gate 14 to enable separate bias. The offset is accomplished by appropriately positioning the top gate mask along the x-axis during the manufacture process.

[0053] Fifth and sixth spacers 64, 66 are disposed adjacent the bottom gate 14 to insulate the bottom gate 14 as needed. In the four terminal device, the sixth spacer 66 separates the bottom gate 14 and the channel 22 from the first local interconnect 32.

[0054] Seventh and eighth spacers 68, 70 are disposed to isolate the transistor 10. The spacers 68, 70 may be extensions of the spacers 48, 50 that surround the transistor 10. The insulating layer 52 surrounds and further isolates the transistor 10.

[0055] Referring to Figure 4, an alternative embodiment of a transistor 100 is shown wherein the bottom gate 14 is electrically isolated by the spacers 64, 66 and the high resistivity layer 16. This embodiment is referenced herein as a floating body

transistor. The top gate 30 extends over the spacers 64, 66 and covers the gate dielectric insulator 28, channel 22, and bottom gate 14. A second local interconnect 60 and an insulator 62 are not required and not present in this embodiment.

[0056] In manufacture, a top gate mask is used that extends over a larger area than the bottom gate 14. The top gate 30 and the bottom gate 14 are aligned relative to one another along the x-axis so that the bottom gate 14 is within the perimeter of the top gate 30.

[0057] Referring to Figure 5, an alternative embodiment of a transistor 110 of the present invention is shown. The transistor 110 is a dynamic threshold (DTMOS) device wherein the top and bottom gates 14, 30 are shorted to one another. The top gate 30 and the bottom gate 14 are disposed in an offset relationship similar to that of Figure 3. The transistor 110 does not include a second local interconnect 60 or an insulator 62. Instead, the first local interconnect 32 occupies the space formerly reserved for the second local interconnect 60 and insulator 62 and couples with both the top and bottom gates 14, 30. An advantage of the present invention is that the DTMOS application occupies the same footprint as a three terminal device and incurs no layout penalty.

[0058] Positioning the top gate and bottom gate masks in the x-axis relative to one another provides a four terminal device, a floating body transistor, or a DTMOS MOSFET. As such, the present invention provides a flexible transistor architecture that is adjusted by mask positioning to create different transistor configurations.

[0059] Referring to Figures 6, 7, and 8, schematic representations of the transistor embodiments corresponding to Figures 3, 4, and 5 are shown. Figure 6 illustrates a four terminal device that provides independent bias to the top gate 30 and the bottom gate 14. Figure 7 illustrates a floating body transistor wherein the

bottom gate 14 is isolated and does not have a terminal connection. Figure 8 illustrates a DTMOS device wherein the bottom gate 14 and the top gate 30 are shorted to one another. As is well known in the art, each device represented in Figures 6-8 has specific uses that are suitable for different applications.

[0060] Referring to Figure 9, a cross-sectional view of an alternative embodiment of a transistor 200 of the present invention is shown. The transistor 200 is similar to that previously illustrated in Figure 1, in that the source 18 and drain 20 each include a respective extension 24, 26 coupled to a channel 202. As before, spacers 44, 46 are disposed between the majority of the source 18 and drain 20 and the channel 202 to reduce the field effect on the channel 202.

[0061] The channel 202 is U-shaped, which increases the channel length and the electron flow path. The increased channel length allows for greater gate control over the channel 202. Thus, the gate control over the channel 202 is significantly improved at the expense of an increased channel length.

[0062] A gate dielectric insulator 204 is disposed on the channel 202 and may also be U-shaped as it conforms to the channel 202. Alternatively, the gate dielectric insulator 204 may be shaped in other forms and still be within the scope of the present invention.

[0063] Other elements of the transistor 200 operate in a similar fashion to that previously described above. A cross-sectional view of the length of the transistor 200 would be similar to that shown in Figure 3. As can be appreciated, the view shown in Figure 3 would be adjusted to account for the position of the channel 202 and gate dielectric insulator 204.

[0064] Referring to Figure 10, there is shown a cross-sectional view of an alternative embodiment of a transistor 300 of the present invention. As illustrated,

the transistor 300 is similar to the embodiment of Figure 1, and primarily differs in the shape of the source 302, drain 304, and their corresponding extensions 306, 308. The source 302 and drain 304 are vertically aligned closer to the channel 22 than in the previous embodiment. As such, the extensions 306, 308 are shorter and extend primarily in a horizontal direction to couple with the channel 22. The shorter extensions 306, 308 reduce the resistance in the electron flow path.

[0065] As in previous embodiments, spacers 44, 46 are disposed between the channel 22 and the majority of the source 302 and drain 304. Accordingly, the channel 22 is partially shielded to reduce the field effect and provide superior gate control.

[0066] Referring to Figure 11, a cross-sectional view of an alternative embodiment of a transistor 400 of the present invention is shown. The transistor 400 is similar to that of Figure 10 with the primary difference being the shape of the channel 402. The channel 402 is in a U-shape similar to the embodiment of Figure 9. The increased channel length improves the gate control while increasing the resistance experienced in the flow path. A gate dielectric insulator 404 is disposed on the channel 402 and may have a planar configuration as shown, or have a U shape.

[0067] Transistors 200, 300, 400 may also be referred to as a configurable transistor in that the alignment of the top gate and bottom gate determines the terminal connections, electrical behavior, and threshold voltage of the device. Thus, the transistors 200, 300, 400 may be embodied as a four terminal device, floating body transistor, or a DTMOS MOSFET, as explained in reference to Figures 3 to 8.

[0068] Referring to Figures 12 to 20, a method for manufacturing the transistor 10 of Figure 1 is shown. One of skill in the art will appreciate that various processes

may be used to create a transistor structure, and are included within the scope of the invention. The method described herein is exemplary and is for illustrative purposes only.

[0069] Referring more specifically to Figure 12, a cross-sectional view of preliminary layers used in fabrication is shown. The transistor 10 includes a substrate layer 12 that may be formed of any number of resistive materials suitable for the present invention. In one implementation, the substrate 12 may include a lower layer of silicon and a buried oxide layer disposed thereon. A high resistivity layer 16, such as crystalline silicon, is formed on the substrate layer 12 by any known method. A source/drain layer 500 is formed on the substrate layer 12, and may also include crystalline silicon that is doped with ion implants to form a N+ material. The source/drain layer 500 may be subjected to a metalization step wherein a silicide is applied and removed to improve performance. Typically, a silicide such as TiSi, MoSi, or CoSi, is sputtered onto the surface of the source/drain layer 500 and then stripped away to increase electron mobility. A dielectric layer 502 is formed on the source/drain layer 500. The dielectric layer 502 includes either silicon nitride or silicon oxide.

[0070] Referring to Figure 13, a trench is formed in the dielectric layer 502 and the source/drain layer 500. The trench is etched in accordance with an applied trench mask to form the main bodies 23, 25, of the source 18, and drain 20.

[0071] Referring to Figure 14, a solid source doping technique is used to form the source and drain extensions 24, 26. A layer of a heavily doped solid is formed within the trench 504 and then etched to provide doped sidewalls 506. The doped sidewalls 506 act as a source to infuse a dopant to the high resistivity layer 16. The regions of the high resistivity layer 16 proximate to the sidewalls 506 become the N+

source and drain extensions 24, 26. In an alternative technique, the extensions 24, 26 may be formed by conventional ion implantation.

[0072] Referring to Figure 15, the doped sidewalls 506 are removed. A dielectric layer is formed within the trench 504 and etched to form a gate dielectric insulator 28 on the trench bottom.

[0073] Referring to Figure 16, a layer of silicon nitride is formed within the trench 504 and etched to form first and second spacers 44, 46.

[0074] In Figure 17, the high resistivity layer 16 is doped with high level ion implants to form a P+ bottom gate 14. The ion implants are directed through the trench 504 to contact the high resistivity 16 and form the bottom gate 14 in the appropriate location. A channel 22 is defined as the proximate area between the bottom gate 14, extensions 24, 26, and gate dielectric insulator 28.

[0075] Referring to Figure 18, a top gate layer 30 is deposited within the trench 504 using any number of methods such as sputtering, evaporation, pulsed laser ablation, oxidation, chemical vapor deposition, electroplating, and other techniques commonly known in the art. The top gate layer is then etched to form the top gate 30 in accordance with a top gate mask. Configuration of the top gate mask and doping of the bottom gate may be altered to manufacture alternative devices such as those shown in Figures 4 and 5. The top gate 30 may also be subjected to a metalization step such as the source/drain layer 500 to mobility performance.

[0076] Referring to Figure 19, a conductive layer is formed within the trench 504 and planarized to form the first local interconnect 32. Although not illustrated in Figure 19, the second local interconnect 60 is disposed adjacent the insulator 62 and in contact with the bottom gate 14 as shown in Figure 3.

[0077] Spacers 48, 50 are formed on the perimeter of the transistor 10 to isolate the transistor 10. Formation of the spacers 48, 50 may occur simultaneously with the formation of spacers 44, 46 as well as simultaneously with the formation of spacers 64, 66, 68, 70. An STI layer 52 is formed proximate to the spacers 48, 50 to further isolate the transistor 10. Formation of the STI layer 52 may occur at any time after formation of the spacers 48, 50. An ILD layer 42 is disposed on the pads 34, 36, local interconnect 32, and STI layer 52, and then planarized.

[0078] Referring to Figure 20, a contact mask is applied to the ILD layer 42, and pads 34, 36 to form wells 508 that provide access to the source 18 and drain 20. A conductive layer is formed in the wells 508 and planarized to create contact layers 38, 40.

[0079] Similar techniques may be employed to manufacture the embodiments shown in Figures 9 to 11. Variances in deposition and etching techniques as well as variances in materials used may be employed and are within the scope of the invention.

[0080] A further advantage of the present invention is its inherent radiation hardness. To limit radiation sensitivity, the pads 34, 36, exterior spacers 48, 50, 68, 70, and high resistivity layer 16 may all be embodied as a nitride. The exterior spacer 48, 50, 68, 70 surround the transistor components. With the addition of the pads, 34, 36, the transistor 10 is encapsulated within nitride to provide a buffer against radiation. Radiation will tend to accumulate within an oxide such as in a buried oxide of the substrate 12. The source 18 and drain 20 are separated from the substrate 12 by the high resistivity layer 16 to limit the effect of accumulated radiation. Remaining radiation effects may be compensated by dynamic control of the bottom gate 14.

[0081] The present invention provides a unique transistor architecture that greatly improves gate control of the channel. The improved gate control is achieved in various embodiments by providing extensions to distance the source and drain, spacers to insulate against the source and drain, and increased channel length. The resulting electron flow path has high mobility and high current drive. The transistor architecture is flexible and may be configured with different terminal connections for different electrical behavior. In one embodiment, the present invention provides a double-gated transistor with independent gate control.

[0082] Referring to Figure 21, a schematic diagram of an embodiment of a SRAM cell 600 is shown. The SRAM cell 600 includes internal MOSFET transistors, including two NMOS transistors 602, 604 and two PMOS transistors 606, 608 that are interconnected to construct a latch and store data. The PMOS transistor 606 couples at its source and drain to a Vdd and to node 1 respectively. The Vdd provides a constant power supply to the SRAM cell 600. The NMOS transistor 602 couples at its source and drain to node 1 and to ground. The gate electrodes 610, 612 of PMOS transistor 606 and NMOS transistor 602 are shorted to one another and to node 2. The PMOS transistor 608 couples at its source and drain to Vdd and to node 2. The NMOS transistor 604 couples at its source and drain to node 2 and to ground. The gate electrodes 614, 616 of PMOS transistor 608 and NMOS transistor 604 are shorted to one another and to node 1.

[0083] The SRAM cell 600 further includes two pass NMOS transistors 618, 620 that are coupled to node 1 and node 2 and Bit Line and inverse Bit Line respectively. The gate electrodes 622, 624 of both pass NMOS transistors 618, 620 are coupled to a Write Line to enable control. The pass NMOS transistors 618, 620 function as switches that open and close access to the SRAM cell 600.

[0084] Write and Read operation of the SRAM cell 600 are performed by executing a sequence of action by external control. A Write operation is performed by first charging the Bit Line and inverse Bit Line with values that are desired to be stored in the SRAM cell 600. Setting the Write Line high performs the actual write operation and the new data is latched into the cell 600. The interconnected transistors 602, 604, 606, 608 force the internal nodes to appropriate voltage levels and maintain a cell state.

[0085] A Read operation is initiated by charging both the Bit Line and inverse Bit Line to a high state. The Write Line is set high to close the pass NMOS transistors 610, 612 and place the value stored in the cell 600 on the Bit Line and inverse Bit Line. If the cell state is low, then current flows across the pass NMOS transistors 610, 612 because the Bit Line and inverse Bit Line are higher.

[0086] The internal transistors 602, 604, 606, 608, as well as the pass transistors 618, 620, are double-gated three terminal devices such as a floating body transistor of Figure 7 or a DTMOS device of Figure 8. The floating body transistor has a top gate electrode to provide the gate control but the bottom gate is unconnected. The DTMOS transistor has both the top gate and bottom gate shorted together to increase gate control and predictability. The DTMOS transistor allows for lower power operation with Vdd being at a relatively low .5 V. The DTMOS transistor is advantageously available at no area penalty. The internal transistors 602, 604, 606, 608 are further configured in accordance with the embodiments shown in Figures 1, 2, 4, 5, 9, 10, and 11 and all of the benefits discussed therein.

[0087] Referring to Figure 22, an alternative embodiment of a SRAM cell 700 of the present invention is shown. The SRAM cell 700 includes internal NMOS transistors 702, 704 and internal PMOS transistors 706, 708 that are embodied as

double-gated four terminal devices similar to that schematically illustrated in Figure 6. The internal transistors 702, 704, 706, 708 are further configured in accordance with the embodiments discussed herein.

[0088] The top gates of each transistor 702, 704, 706, 708 serve as the gate electrodes 710, 712, 714, 716 respectively to enable gate control. The bottom gates 718, 720 of the NMOS transistors 702, 704 are coupled to ground. The bottom gates 722, 724 of the PMOS transistors 706, 708 are coupled to Vdd. Other than the bottom gate connections, the internal transistors 702, 704, 706, 708 are embodied similar to that of Figure 21, with interconnections to provide a latch. Write and Read operations are performed in a similar manner to that previously described.

[0089] The SRAM cell 700 further includes pass NMOS transistors 726, 728 that are also embodied as double-gated four terminal transistors. The pass transistors 726, 728, include top gates 730, 732 that are coupled to the Write Line and bottom gates 734, 736 that are coupled to ground.

[0090] The grounded bottom gates 718, 720, 734, 736 of the transistors 702, 704, 726, 728 increase the inherent radiation hardness of the SRAM cell 700. Radiation tends to accumulate in the lower components of each transistor, and this allows the bottom gates 718, 720, 734, 736 to direct the accumulated radiation to ground.

[0091] The SRAM cells 600, 700 have numerous advantages by including the unique transistor architecture disclosed in Figures 1 to 20 and the accompanying text. The transistor architecture allows for multiple configurations of a double-gated MOSFET, and includes floating body, DTMOS, and four terminal embodiments for different design applications.

[0092] The double-gated MOSFET transistors have Damascene local interconnects 32, 60 for coupling the top gate 14 and bottom gate 30 and

Damascene contact layers 38, 40 for coupling to the source 18 and drain 20. The local interconnects 32, 60 use an "elevator" configuration to couple to the bottom gate 14, and are embedded in an additive process. Using the Damascene technique, the local interconnects 32, 60 are only placed where they are needed within a trench 504. Excess material of the local interconnects 32, 60 that extend beyond the trench 504 are removed by planarization techniques.

[0093] The transistor architecture does not rely on wells fabrication techniques, which provides process simplicity and increased packing density. The top gate 30 and bottom gate 14 are vertically aligned relative to one another for a thin cell design.

[0094] The top gate 30 is formed as one of the last steps in fabrication which advantageously enables use of temperature intolerant gate dielectrics and metals. Accordingly, exotic materials may be used for the top gate 30, such as Pt, without regard for high temperatures. The critical dimension of the top gate 30 is defined by the spacers 44, 46 in the trench 504 and is fully planar. The top gate 30 may be formed of a low resistance gate material (Ti N, W, Mo) with an adjustable work function. Thus, the threshold voltage of the top gate 30 is adjustable, which avoids doping the channel, thereby improving electron mobility and current drive.

[0095] The MOSFET transistors resist radiation damage by separating the source 18 and drain 20 from the buried oxide of the substrate 12, where radiation is accumulated. The high resistivity layer 16 and spacers 44, 46, 48, 50, may all include nitride to separate and encapsulate the source 18, drain 20, bottom gate 14, and top gate 30 and increase radiation resistance. Radiation resistance is further increased in the four terminal embodiment wherein the bottom gate is grounded to sweep away accumulated radiation. Remaining radiation sensitivity may be

compensated by dynamic control of the bottom gate. Dynamic bottom gate compensation allows repair of the threshold voltage after extended radiation exposure.

[0096] The transistor architecture provides a layout for a SRAM cell that is compact and efficient for a given lithography size. The transistor architecture allows for sub-lithographic channel lengths and conventional lithography techniques.

[0097] The transistor architecture provides a raised low resistance source/drain structure by having the source 18 and drain 20 formed on a relatively thick high resistivity layer 16. Conventional structures utilize a SOI layer of approximately 50 nm, whereas the present invention allows for a high resistivity layer 16 of greater than 200 nm. A thick high resistivity layer 16 lowers the resistance of the source 18 and drain 20.

[0098] It will be obvious to those having skill in the art that many changes may be made to the details of the above-described embodiments without departing from the underlying principles of the invention. The scope of the present invention should, therefore, be determined only by the following claims.

[0099] What is claimed is: